Carte station domotique

Ce document sert de récapitulatif concernant les choix technique choisi dans notre schématique.

Partie communication

NRF24L01P : Transmission radio

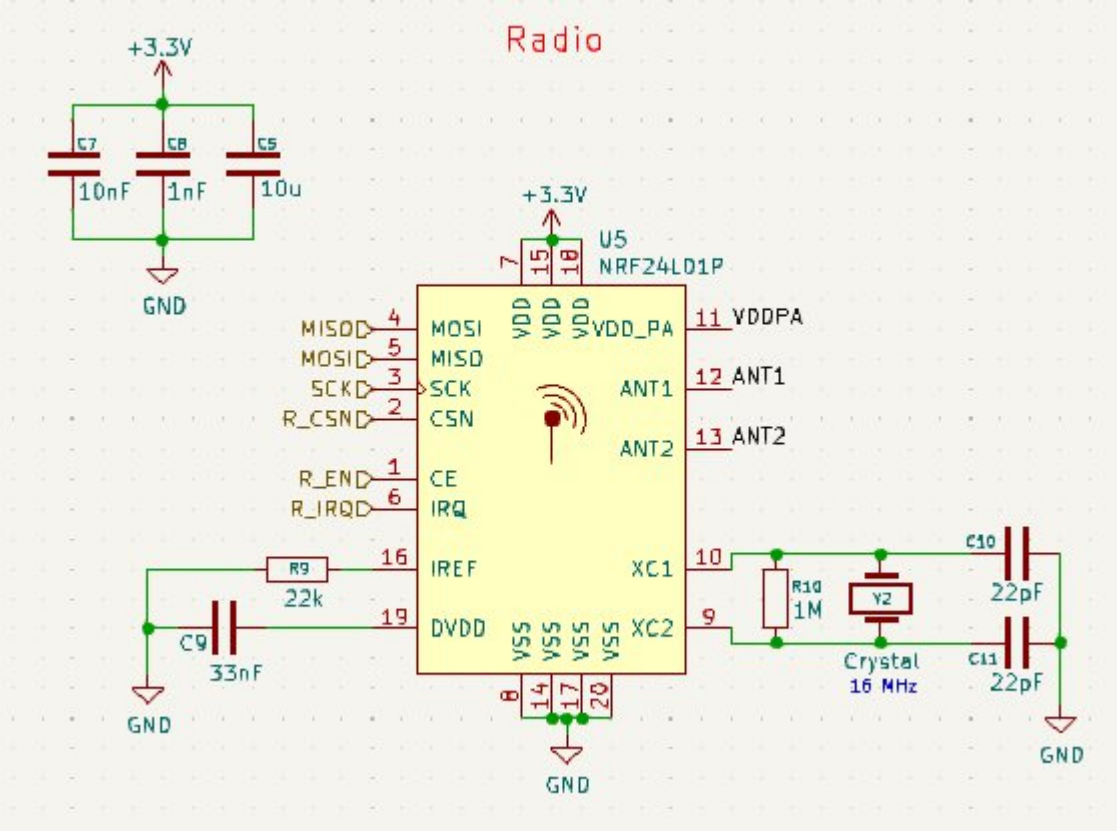


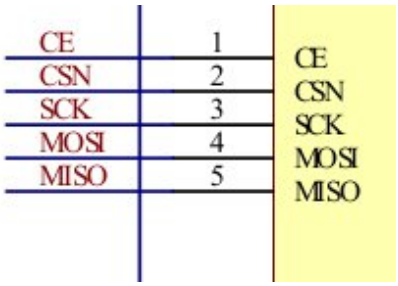
Figure 1 : Schéma application page 69 de la datasheet.

Operating conditions	Minimum	Maximum	Units
Supply voltages			
VDD	-0.3	3.6	V
VSS		0	V

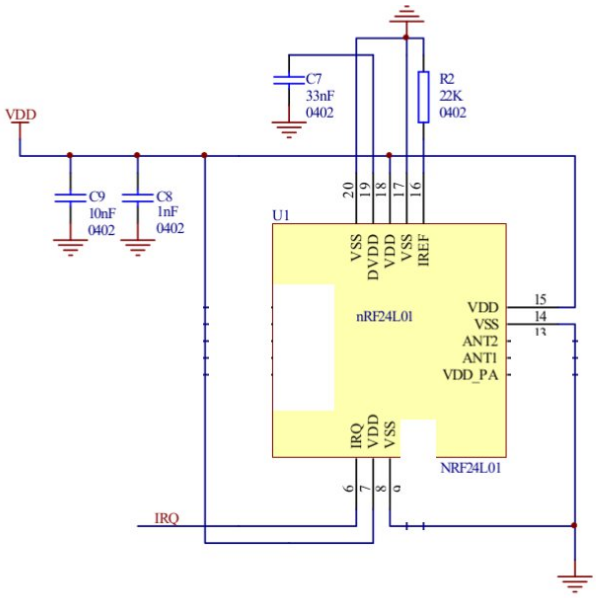
Figure 2 : Table page 12

Ce tableau indique qu'il faut bien utilisé du 3,3V pour alimenter notre composant donc il faudra ajouter un régulateur de tension.

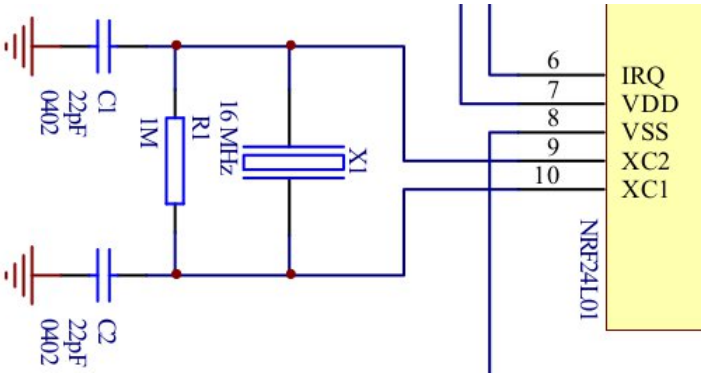
- **Commande**



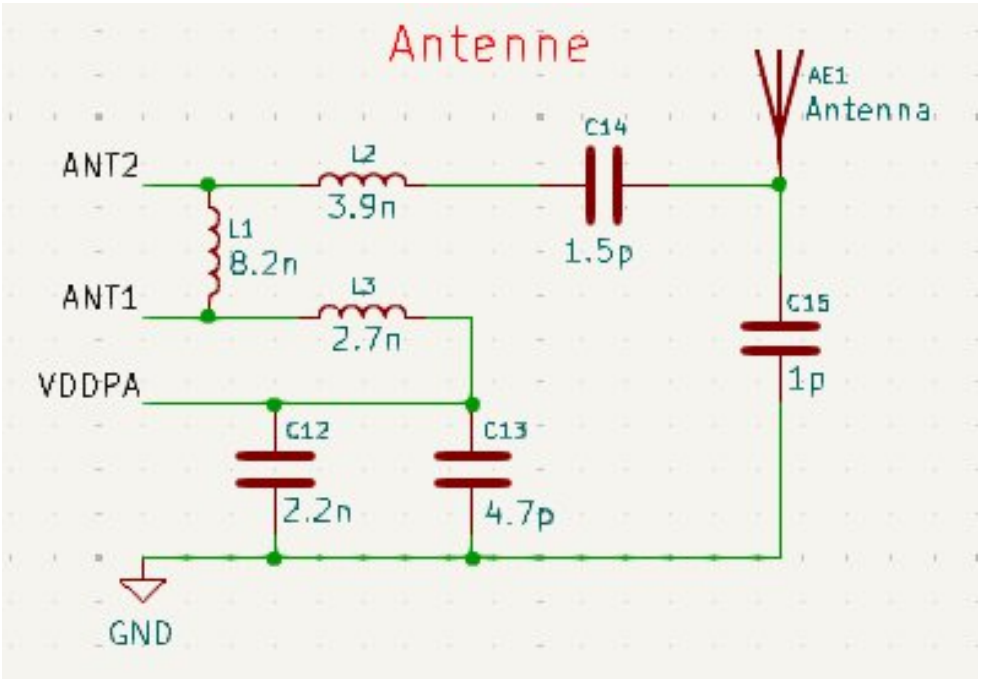
- **Alimentation**

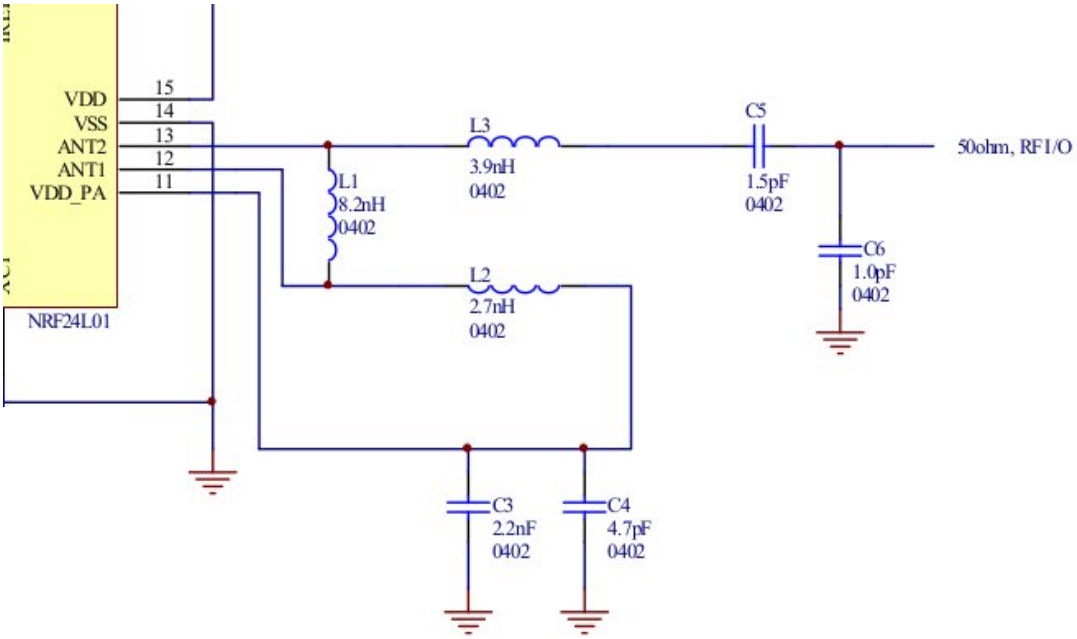


- **Le crystal**



Antenne


Antenne
AE1
Antenna
C14
1.5p
ANT2
L2
3.9n
L1
8.2n
ANT1
L3
2.7n
C15
1p
VDDPA
C12
2.2n
C13
4.7p
GND


VDD
VSS
ANT2
ANT1
VDD_PA
15
14
13
12
11
NRF24L01
L3
3.9nH
0402
C5
1.5pF
0402
50ohm, RF I/O
L1
8.2nH
0402
C6
1.0pF
0402
L2
2.7nH
0402
C3
2.2nF
0402
C4
4.7pF
0402

Partie puissance

LTC3531 : Régulateur de tension

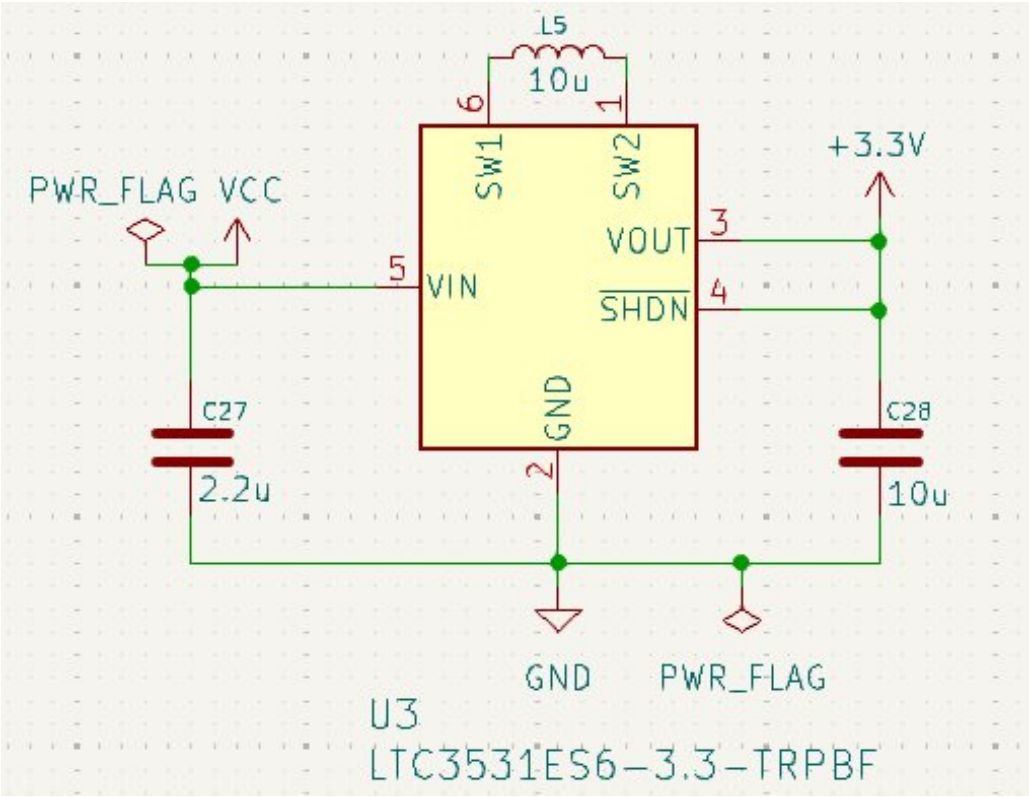


Figure 3 : Schéma kicad LTC3531-3V3

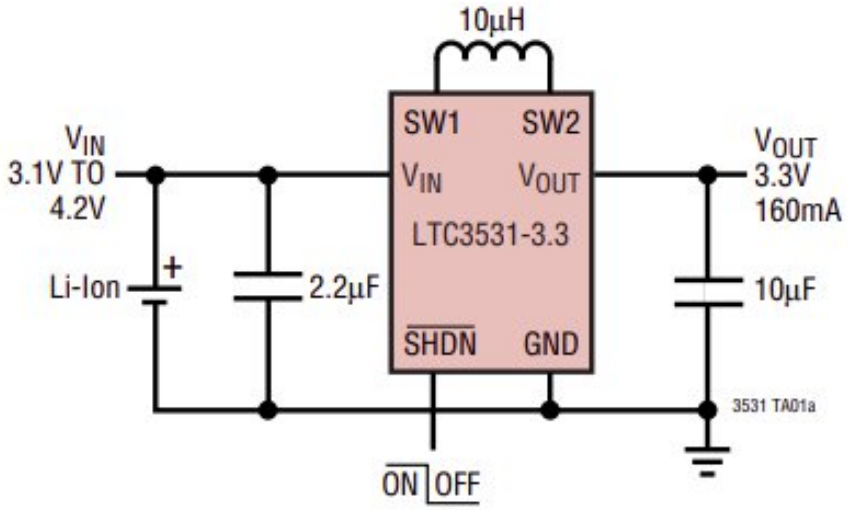


Figure 4 : Schéma application LTC3531-3V3 page 1 de la datasheet

MAX1811 : Chargeur de la batterie

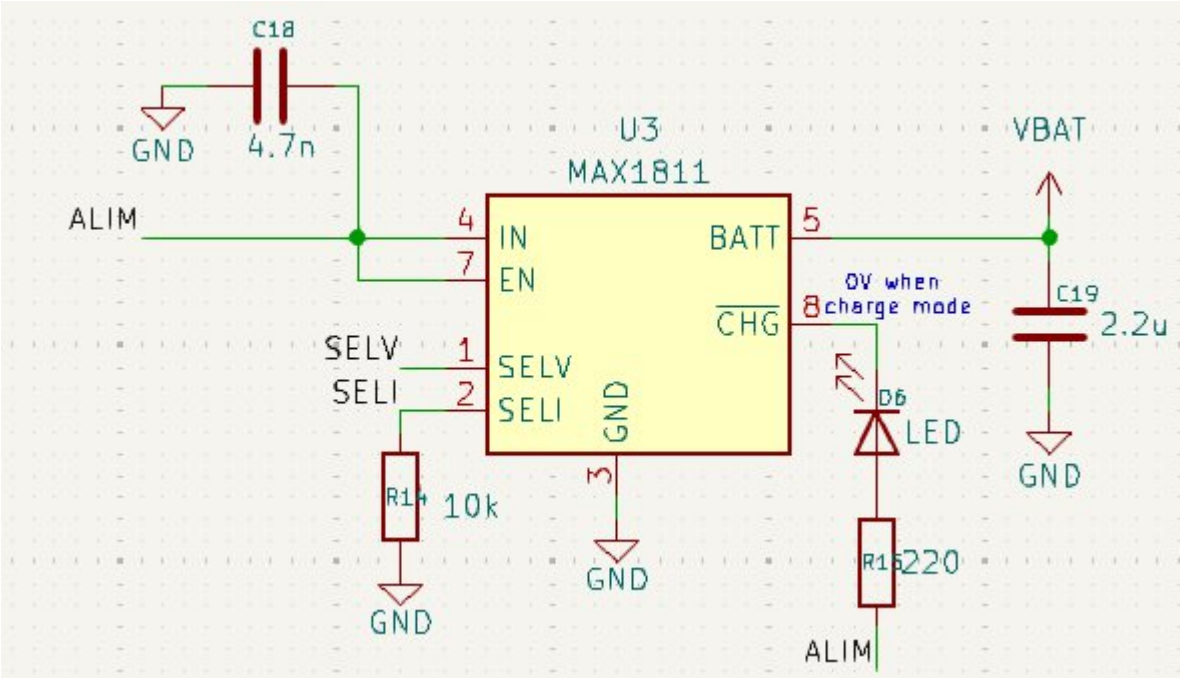


Figure 5 : Notre schéma kicad du MAX1811

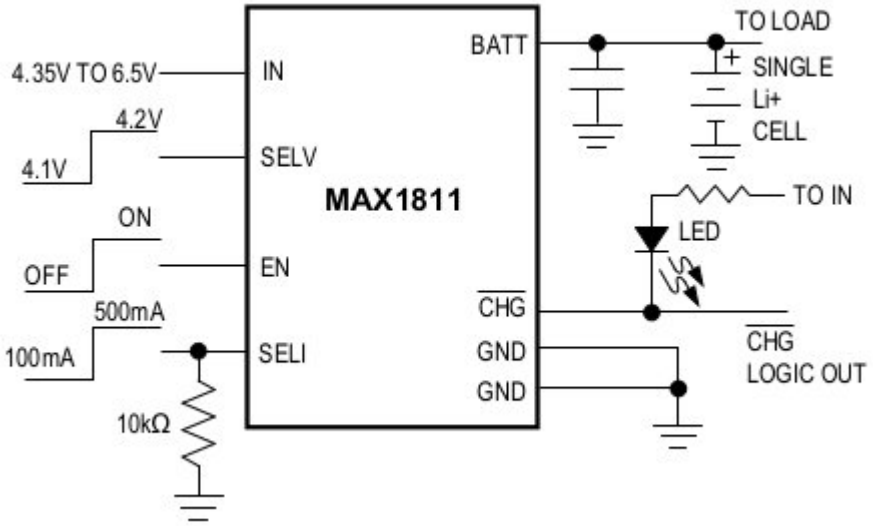


Figure 6 : Référence design MAX1811 de la datasheet page 7

Le schéma donné par la datasheet ne nous donnait pas la valeur de la capacité donc je l'ai cherché sur internet et j'ai trouvé ceci :

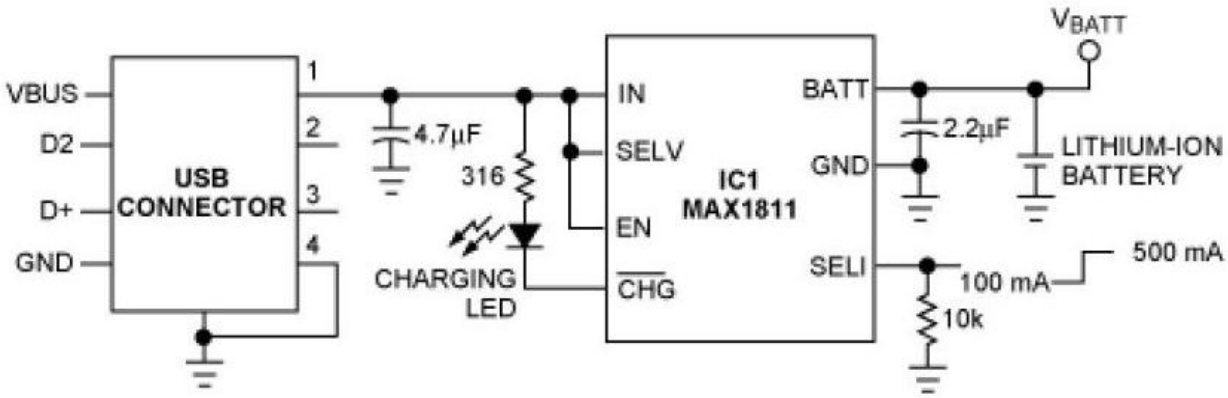
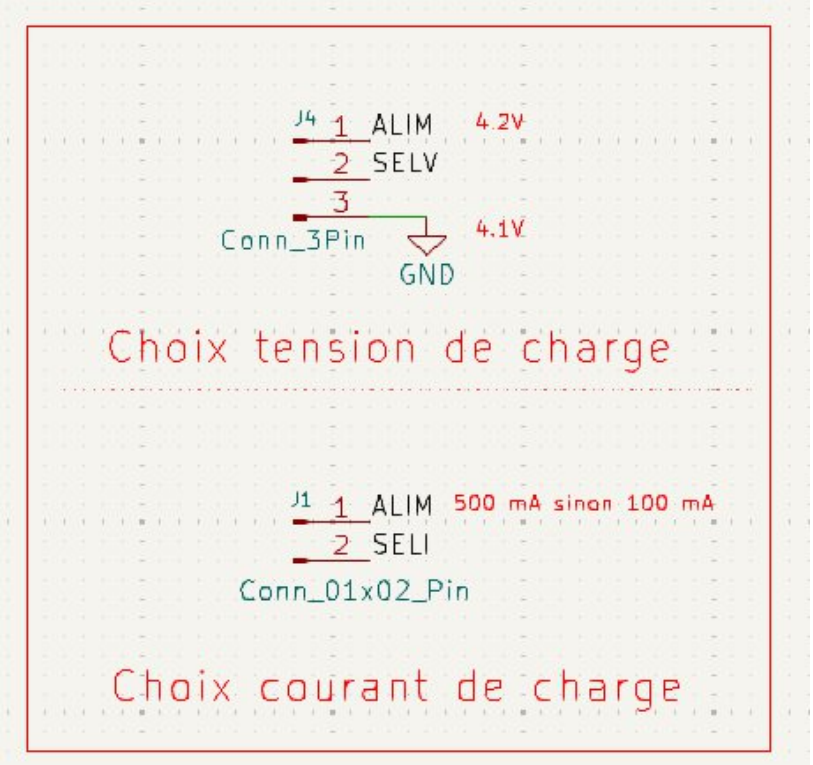


Figure 7 : Schéma design MAX1811

Cette référence design à été trouvé via cette source : https://www.arrow.com/en/reference-designs/33-5v-1-cell-lithium-ion-battery-charger-for-portable/f0a648688917a898ee3ca56232c46f0f8a2e41bb6c

Le choix de l'ampérage et de la tension de charge se fera à la main via des jumpers :



Partie écran

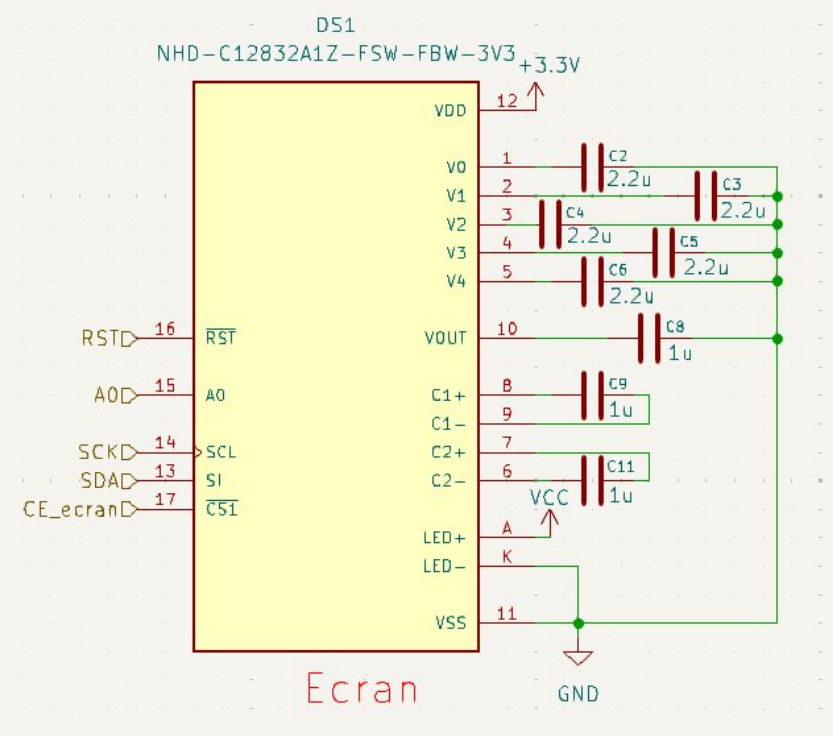


Figure 8 : Notre schéma kicad pour l'écran NHD

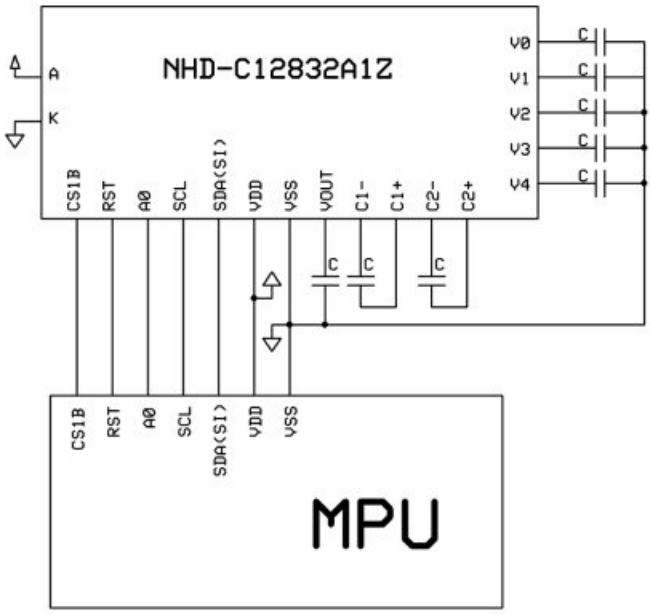


Figure 9 : Référence design NHD-C12832A1Z de la datasheet page 4

ATMEGA32U4 : Microcontrôleur

- **Programmation de l'ATMEGA32U4**

true Read-While-Write operation. By combining an 8-bit RISC CPU with In-System Self-Programmable Flash on a monolithic chip, the device is a powerful microcontroller that provides a highly flexible and cost effective solution to many embedded control applications.

Page 5

This concept enables instructions to be executed in every clock cycle. The program memory is In-System Reprogrammable Flash memory.

Page 9

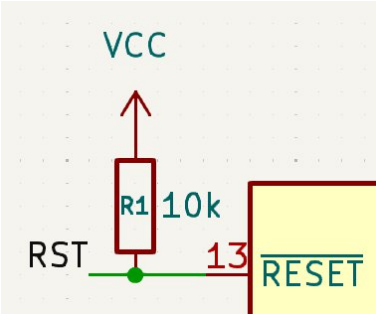
In-System Reprogrammable Flash Program Memory

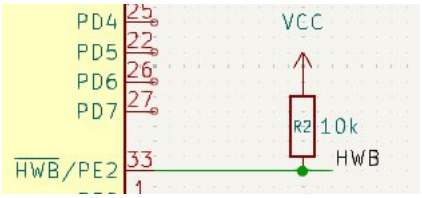
The device contains 16/32K bytes On-chip In-System Reprogrammable Flash memory for program storage. Since all AVR instructions are 16 or 32 bits wide, the Flash is organized as 16K x 16. For software security, the Flash Program memory space is divided into two sections, Boot Program section and Application Program section.

The Flash memory has an endurance of at least 100,000 write/erase cycles. The device Program Counter (PC) is 16 bits wide, thus addressing the 32K program memory locations. The operation of Boot Program section and associated Boot Lock bits for software protection are described in detail in "Memory Programming" on page 353. "Memory Programming" on page 353 contains a detailed description on Flash data serial downloading using the SPI pins or the JTAG interface.

Page 18

- **RESET / HWB**





RST et HWB sont ensuite relié à un bouton qui fait contacte avec une masse pour activer ou non le mode en fonction de ce que souhaite l'utilisateur.

- **Crystal**

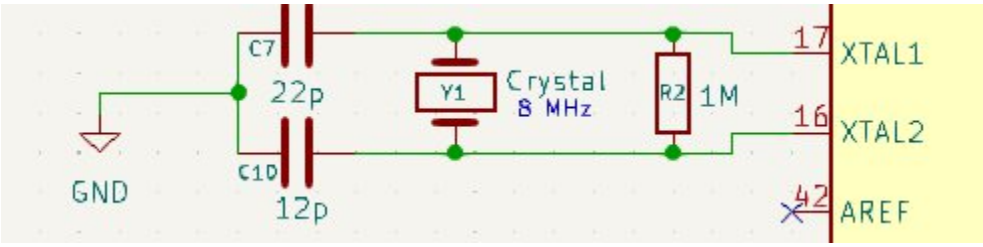


Figure 10 : Schéma kicad de la partie crystal du microcontroleur

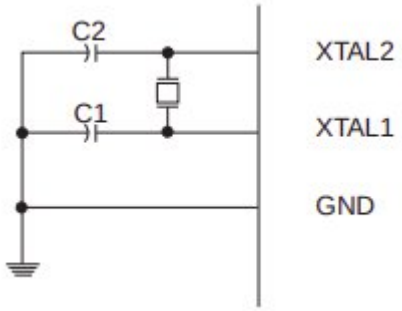


Figure 11 : Schema de la datasheet page 30

Frequency Range[1] [MHz]	CKSEL3..1	Recommended Range for Capacitors C1 and C2 [pF]
0.4 - 0.9	100[2]	–
0.9 - 3.0	101	12 - 22
3.0 - 8.0	110	12 - 22
8.0 - 16.0	111	12 - 22

Figure 12 : Table de la datasheet page 30

Le crystal à notre disposition est de 16 MHz ou de 8 MHz. Ce qui implique d'utiliser C1 et C2 à 12 et 22 pF.

- **Maximum Frequency**
  - **8MHz at 2.7V - Industrial range**
  - **16MHz at 4.5V - Industrial range**

Figure 13 : Information dans la datasheet page 2

Le choix entre 8 ou 16 MHz se fera ensuite en fonction de l'usage. Ici on alimente le microcontrôleur en dessous de 4,5V donc on aura un quartz de 8 MHz

- **USB A**

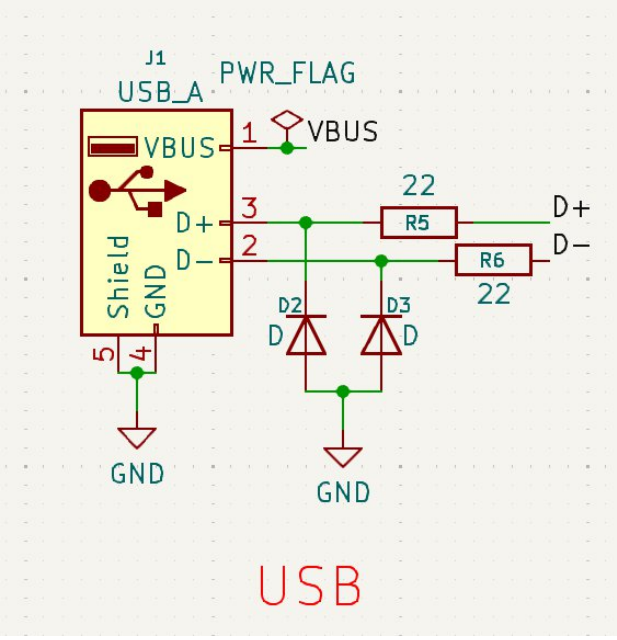


Figure 21-6. Typical Self Powered Application with 3.0V to 3.6 I/O

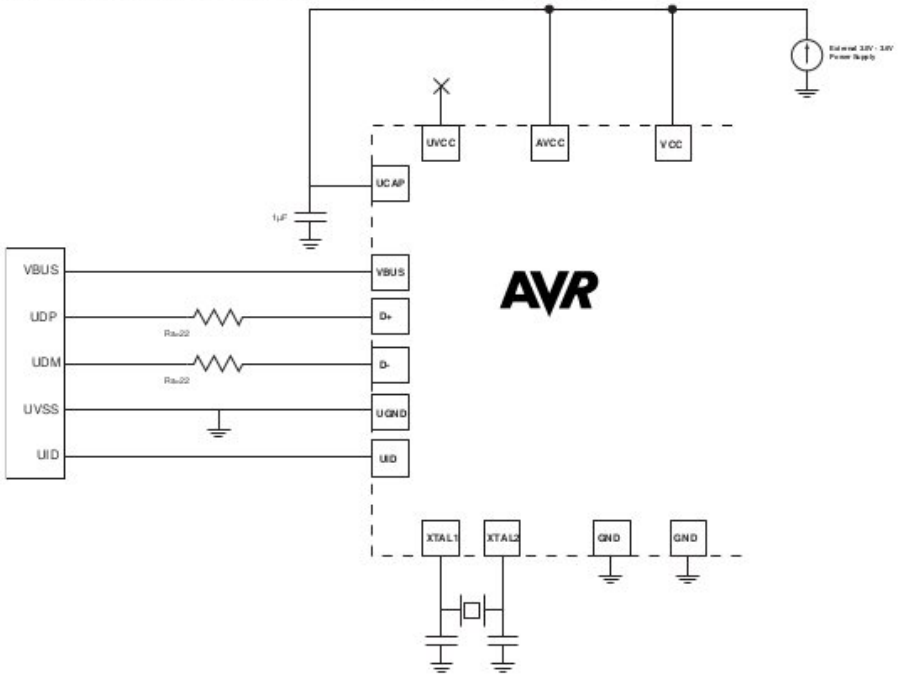
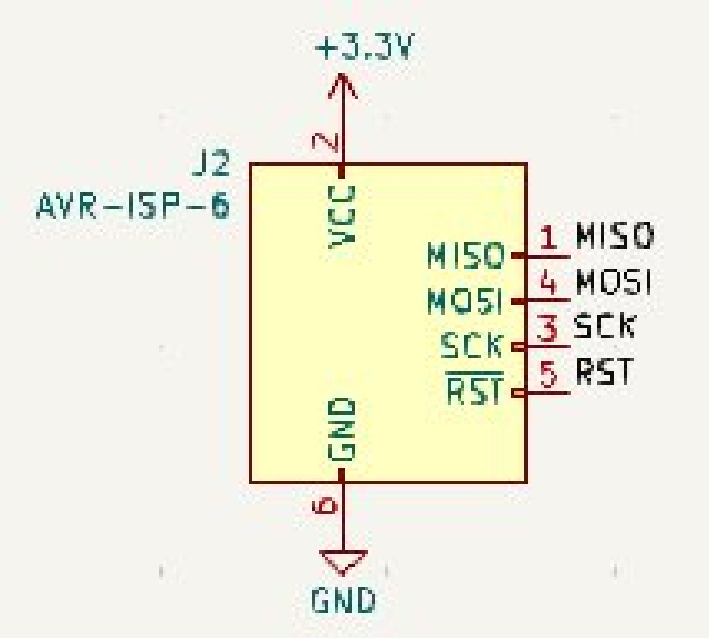


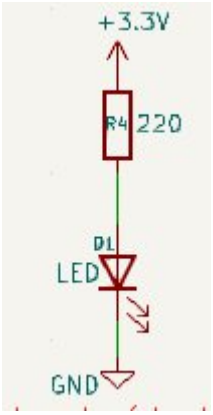
Figure 14 : Datasheet page 258

Concernant la liaison USB, UCAP doit être relié avec un condensateur de 1uF.

- **Connecteur ISP**

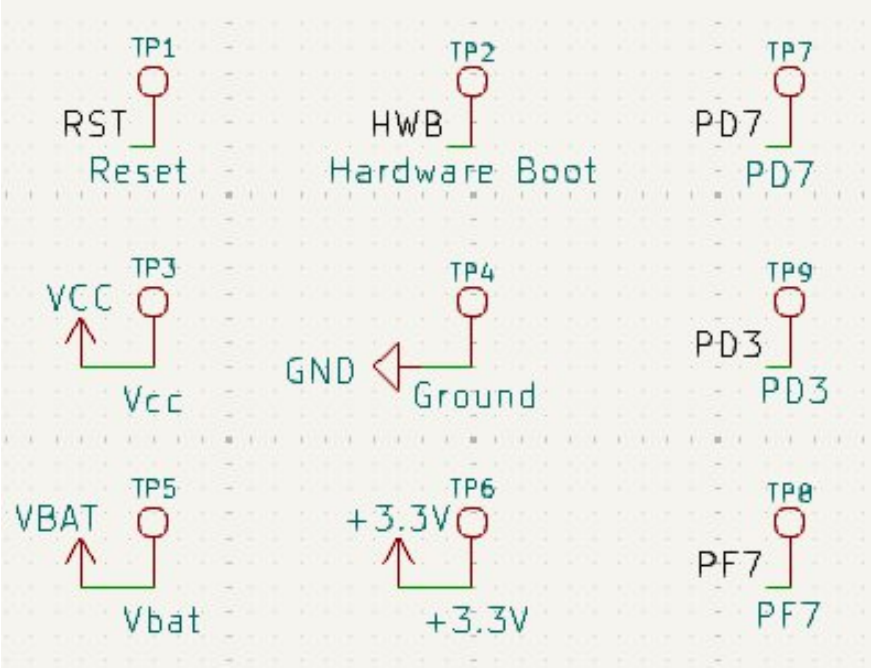


- **LED d’alimentation**



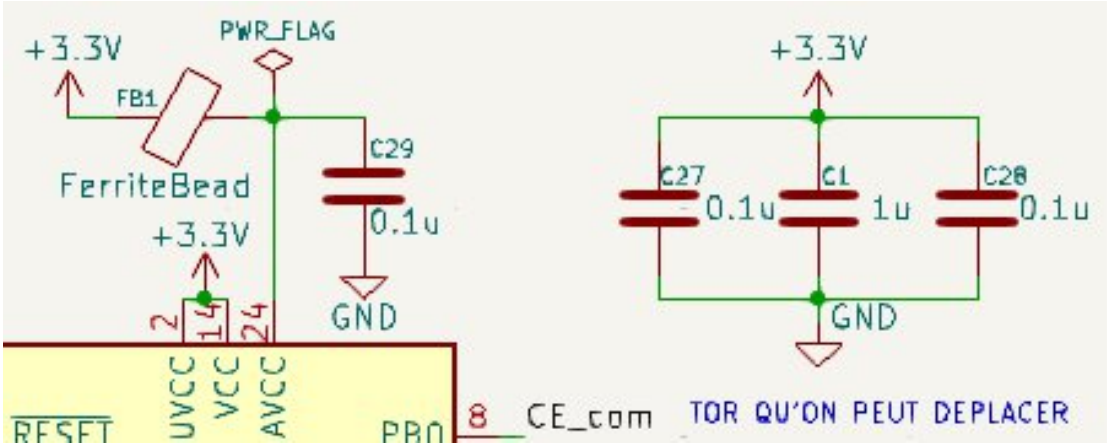
C’est toujours sympa de voir si ça carte est correctement alimenté.

- **Test point**



Permet de vérifier facilement toutes les tensions via des test points.

- **Alimentation**

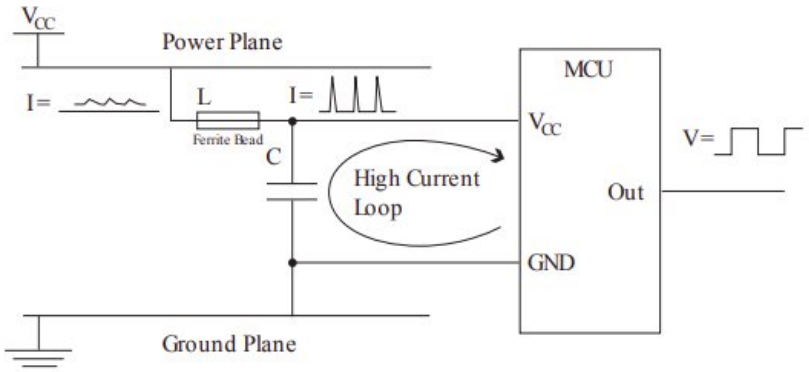


Ajout d'une ferrite et d'un condensateur. Permet de filtrer le bruit.

Ces informations sont recommandés par le constructeur. *(Cf. AVR042)*

A la page 5 on retrouve ce schéma :

Figure 2-2. Decoupling with Series Inductor



In Atmel AVR devices where power and ground lines are placed close together there will be better decoupling than the devices with industry standard pin-out. In industry standard pin-out, the power and ground pins are placed in opposite corners of the DIP package. This disadvantage can be overcome by placing decoupling capacitors very close to the die. For devices with multiple pairs of power and ground pins, it is essential that there is a decoupling capacitor for every pair of pins.

The main power supply should also have a tantalum or ceramic capacitor to stabilize it.

Ce schéma nous montre comment éviter les bruits parasites via le placement d’une ferrite et d’une capacité.

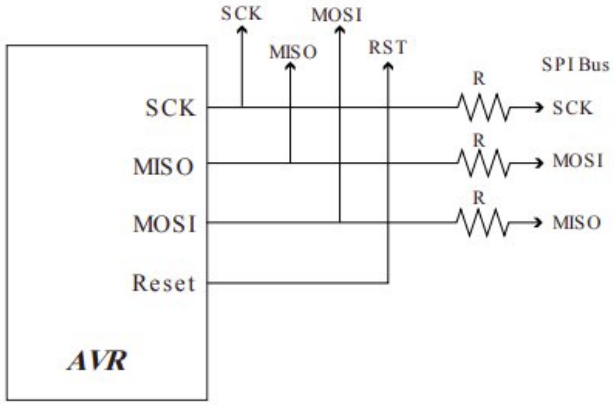
Pour les capacités de découplage il est recommandé par le constructeur de mettre 1 capacité de 100nF pour chaque pair VCC/GND

- **Liaison SPI**

PB3	PDO/MISO/PCINT3 (Programming Data Output or SPI Bus Master Input/Slave Output or Pin Change Interrupt 3)
PB2	PDI/MOSI/PCINT2 (Programming Data Input or SPI Bus Master Output/Slave Input or Pin Change Interrupt 2)
PB1	SCK/PCINT1 (SPI Bus Serial Clock or Pin Change Interrupt 1)
PB0	$\overline{SS}$/PCINT0 (SPI Slave Select input or Pin Change Interrupt 0)

Figure 15 : Table page 74 de la datasheet

Figure 4-2. Connecting the SPI Lines to the ISP Interface



Note:

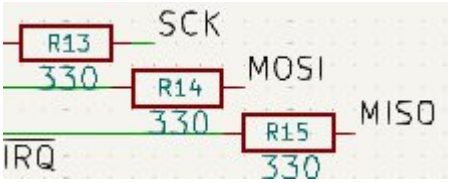
1. These typical values are used to limit the input current to 10mA for a supply voltage (V_{CC}) of 3.3V. It may vary depending on the programmer/debugger used and requirements of specific hardware design.
2. The AVR will never drive the SPI lines in a programming situation. The AVR is held in RESET to enter programming mode, which puts all AVR pins to tri-states.

U = R * I

3.3V = R * 0.01 A

R = 3,3V / 0.01 = 330 Ohms

C’est pourquoi nous avons ajouté ces résistances sur nos broches SPI.



- **Liaison I2C**

SDA et SCL :

PD3	$\overline{INT3}$/TXD1 (External Interrupt3 Input or USART1 Transmit Pin)
PD2	$\overline{INT2}$/RXD1 (External Interrupt2 Input or USART1 Receive Pin)
PD1	$\overline{INT1}$/SDA (External Interrupt1 Input or TWI Serial DAta)
PD0	$\overline{INT0}$/SCL/OC0B (External Interrupt0 Input or TWI Serial CLock or Output Compare for Timer/Counter0)

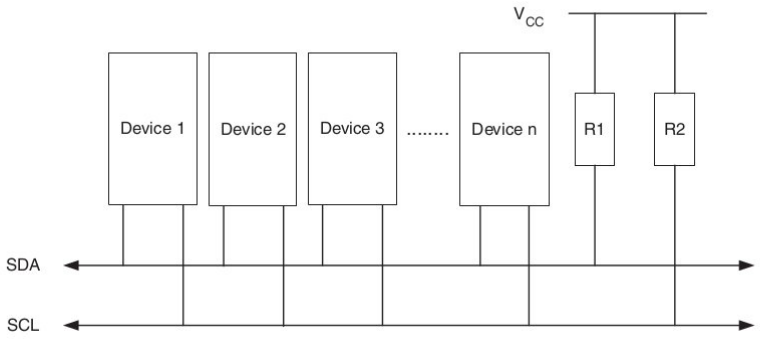
Figure 16 : Table de la page 78

Des résistances à rajouter sur SDA et SCL ?

20.2 2-wire Serial Interface Bus Definition

The 2-wire Serial Interface (TWI) is ideally suited for typical microcontroller applications. The TWI protocol allows the systems designer to interconnect up to 128 different devices using only two bi-directional bus lines, one for clock (SCL) and one for data (SDA). The only external hardware needed to implement the bus is a single pull-up resistor for each of the TWI bus lines. All devices connected to the bus have individual addresses, and mechanisms for resolving bus contention are inherent in the TWI protocol.

Figure 20-1. TWI Bus Interconnection



P225

La table des types des pins :

Table 10-2. Generic Description of Overriding Signals for Alternate Functions

Signal Name	Full Name	Description
PUOE	Pull-up Override Enable	If this signal is set, the pull-up enable is controlled by the PUOV signal. If this signal is cleared, the pull-up is enabled when {DDxn, PORTxn, PUD} = 0b010.
PUOV	Pull-up Override Value	If PUOE is set, the pull-up is enabled/disabled when PUOV is set/cleared, regardless of the setting of the DDxn, PORTxn, and PUD Register bits.
DDOE	Data Direction Override Enable	If this signal is set, the Output Driver Enable is controlled by the DDOV signal. If this signal is cleared, the Output driver is enabled by the DDxn Register bit.
DDOV	Data Direction Override Value	If DDOE is set, the Output Driver is enabled/disabled when DDOV is set/cleared, regardless of the setting of the DDxn Register bit.
PVOE	Port Value Override Enable	If this signal is set and the Output Driver is enabled, the port value is controlled by the PVOV signal. If PVOE is cleared, and the Output Driver is enabled, the port Value is controlled by the PORTxn Register bit.
PVOV	Port Value Override Value	If PVOE is set, the port value is set to PVOV, regardless of the setting of the PORTxn Register bit.
PTOE	Port Toggle Override Enable	If PTOE is set, the PORTxn Register bit is inverted.
DIEOE	Digital Input Enable Override Enable	If this bit is set, the Digital Input Enable is controlled by the DIEOV signal. If this signal is cleared, the Digital Input Enable is determined by MCU state (Normal mode, sleep mode).
DIEOV	Digital Input Enable Override Value	If DIEOE is set, the Digital Input is enabled/disabled when DIEOV is set/cleared, regardless of the MCU state (Normal mode, sleep mode).
DI	Digital Input	This is the Digital Input to alternate functions. In the figure, the signal is connected to the output of the schmitt trigger but before the synchronizer. Unless the Digital Input is used as a clock source, the module with the alternate function will use its own synchronizer.
AIO	Analog Input/Output	This is the Analog Input/output to/from alternate functions. The signal is connected directly to the pad, and can be used bi-directionally.

Figure 17 : Page 73 de la datasheet